Consumer Microcircuits Limited
COMMUNICATION SEMICONDUCTORS

CMX625
ISDN TA POTS Interface

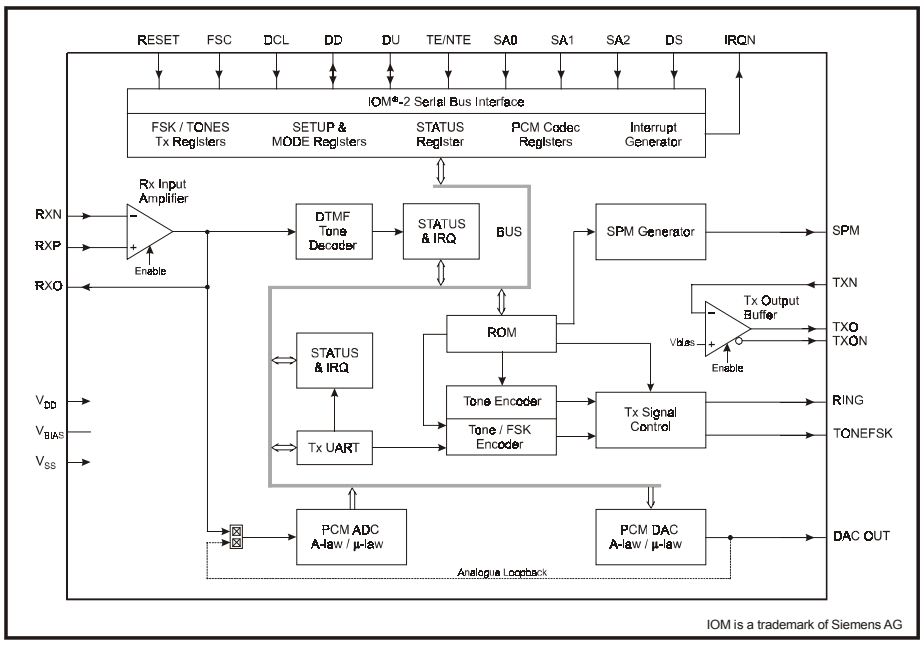
D/625/2 July 2001 Advance Information

Features

- SPM and Ringing Voltage Generators
- Integrated DTMF Decoder/Encoder
- V.23/Bell 202 FSK/Tone Generator
- Selectable A-Law/µ-Law PCM Codec
- IOM-2 Interface Terminal Mode and Non-Terminal Mode (Line Card Mode)

Applications

- ISDN NTUs with Analogue Ports
- ISDN Line Cards
- Wireless Local Loop Termination Cards
- ISDN Terminals with Additional POTS Ports
- PC based ISDN Cards with Telephone Ports
- Billing/SPM Systems



2.7V
LOW POWER OPERATION

1.1 Brief Description

The CMX625 is an integrated telecom tone generator, DTMF encoder/decoder and PCM Codec-Filter designed for ISDN interfaces, Wireless Local Loop and other digitised speech systems. The tone generator covers a wide range of pre-programmed tones used in analogue phone systems. Three outputs are provided: Ringing signals, In-band tones or FSK data, and 12kHz/16kHz Subscriber Metering pulses.

The PCM Codec-Filter performs voice digitisation and reconstruction and incorporates band limiting and smoothing with selectable A-law or µ-law companding following ITU-T recommendation G.711. The DTMF decoder presents the serial bus interface with the DTMF dialling information received from the telephone user and the tone generator sends the appropriate DTMF tones to this POTS interface. Other tone standards supported are: Fax and Modem ‘answer’ and ‘originate’, ITU-T ‘R1’ and ‘R2’ signals, dual tones for CIDCW and 'On-Hook' signalling systems and sufficient tones for simple melody generation.

The IOM®-2 (ISDN Oriented Modular revision 2) industry standard serial bus provides the digital interface to other telecommunications ICs and supports both Terminal and non-Terminal (or Line Card) modes. The CMX625 is compatible with the CMX635 ISDN Subscriber Processor and can be used to provide the additional POTS port. It is available in both DIP and SSOP packages.

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1.2 Block Diagram

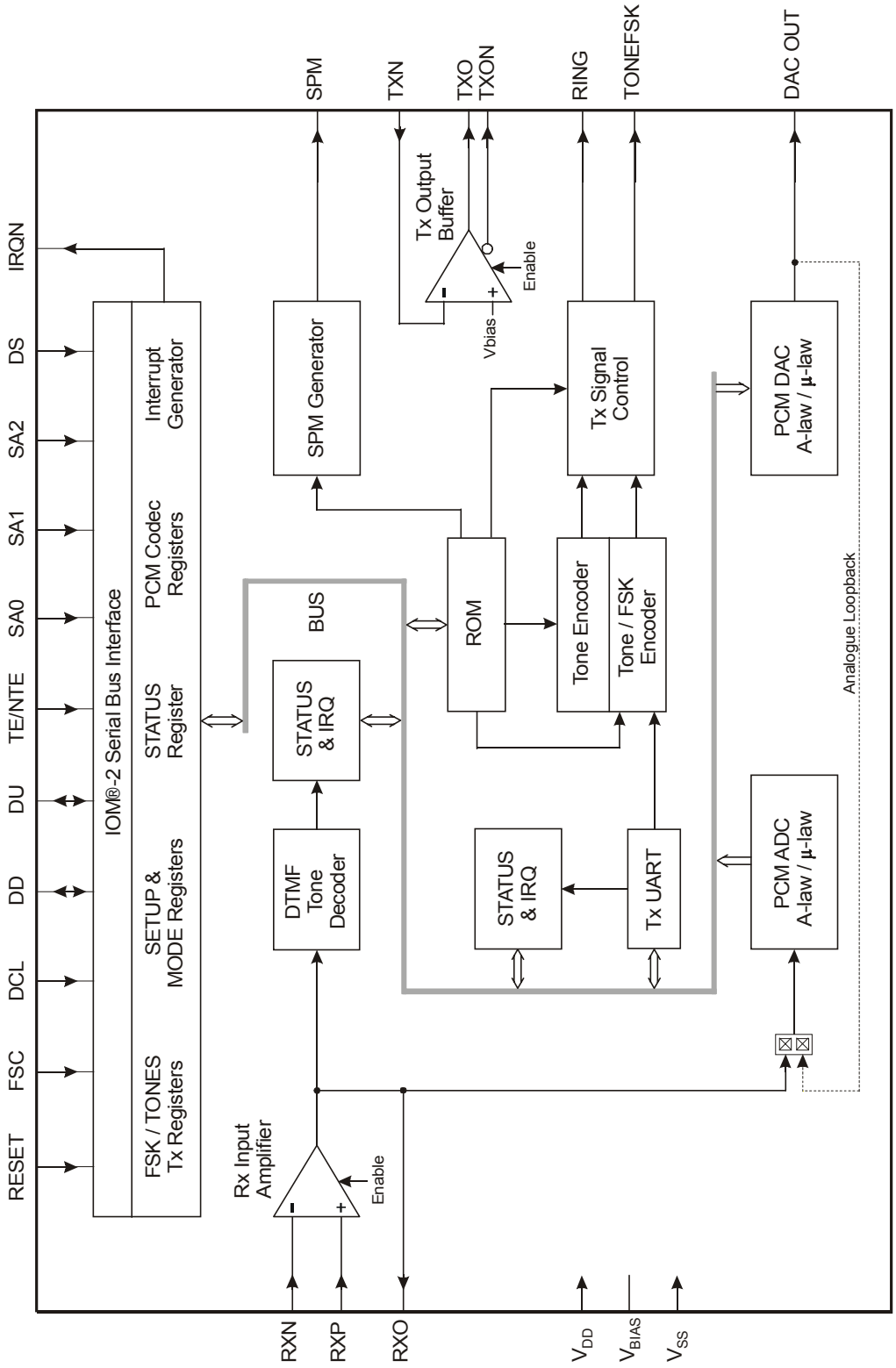


Figure 1 Block Diagram

1.3 Signal List

CMX625 D5/P4	Signal		Description
Pin No.	**Name**	**Type**	
1	FSC	I/P	The IOM-2 Frame Synchronisation Clock. This is an 8kHz clock indicating the start of the frame. FSC is generated by the upstream device. See section 1.5.1, 1.5.2 and 1.5.3.
2	DCL	I/P	The IOM-2 Data Clock. It is used to clock data on and off the bus and operates at 1.536MHz for Terminal mode (TE) or 4.096MHz for non-Terminal mode (non-TE or Line Card mode). DCL is generated by the upstream device. When the bus is deactivated, DCL is held in a low state. See section 1.5.1, 1.5.2 and 1.5.3.
3	DD	BI	The IOM-2 Data Downstream, receives data from the network. When the bus is deactivated or when data is not being transmitted, DD is high impedance. The IC Channel Bus Reversal (TE mode only) allows IC1 and IC2 data to be transmitted on the DD pin. See section 1.5.1, 1.5.2, 1.5.3 and 1.5.6. An external pull-up resistor is required.
4	DU	BI	The IOM-2 Data Upstream, transmits data to the network. When the bus is deactivated or when data is not being transmitted, DU is high impedance. The IC Channel Bus Reversal (TE mode only) allows IC1 and IC2 data to be received on the DU pin. See section 1.5.1, 1.5.2, 1.5.3 and 1.5.6. An external pull-up resistor is required.
5	TE/NTE	I/P	The IOM-2 two modes of operation: TE = 0 selects Terminal mode. NTE = 1 selects Non-Terminal mode or Line Card mode. See section 1.5.1, 1.5.2 and 1.5.3.
6	SA0	I/P	) The IOM-2 Slot Address, provides one of 8 unique
7	SA1	I/P	) addresses. It allows the device to be individually
8	SA2	I/P	) addressed when more than one device is connected) to the IOM-2 bus. See section 1.5.2 and 1.5.3.
9	DS	I/P	The IOM-2 Device Select pin (NTE mode only). Allows two CMX625 devices sharing a Slot Address to be individually addressed. DS = 0 selects device one. DS = 1 selects device two. See section 1.5.2 and 1.5.3.
10	RESET	I/P	The external reset pin clears all the registers. (RESET=1)
11	IRQN	O/P	A 'wire-Orable' output Interrupt Request. This output is pulled down to V_{SS} when active and is high impedance when inactive. An external pull-up resistor is required.

CMX625 D5/P4	Signal		Description
Pin No.	**Name**	**Type**	
12	V_{SS}	Power	The negative supply rail (ground).
13	RXP	I/P	The non-inverting input of the receive op-amp.
14	RXN	I/P	The inverting input of the receive op-amp.
15	RXO	O/P	The output of the receive op-amp.
16	V_{BIAS}	O/P	An internally generated bias voltage of $V_{DD}/2$, except when the device has been reset, V_{BIAS} will discharge to V_{SS}. It should be decoupled to V_{SS} by a capacitor mounted close to the device pins.
17	TONEFSK	O/P	The sinewave output of the Tones and FSK signal generators.
18	TXO	O/P	The output of the buffer amplifier.
19	TXN	I/P	The inverting input to the buffer amplifier.
20	TXON	O/P	The inverted output of the buffer amplifier.
21	DAC OUT	O/P	The output from the digital-to-analogue converter.
22	RING	O/P	The square, trapezoidal and sinusoidal wave output from the Ringing Signal Generator.
23	SPM	O/P	The sinewave output of the SPM signal generator.
24	V_{DD}	Power	The positive supply rail. Levels and thresholds within the device are proportional to this voltage. It should be decoupled to V_{SS} by a capacitor mounted close to the device pins.

Notes: I/P = Input
O/P = Output
BI = Bi-directional
N/C = No (external) Connection

This device is capable of detecting and decoding small amplitude signals. To achieve this V_{DD} and V_{BIAS} decoupling and protecting the receive path from extraneous in-band signals are very important. It is recommended that the printed circuit board is laid out with a ground plane in the CMX625 area to provide a low impedance connection between the V_{SS} pin and the V_{DD} and V_{BIAS} decoupling capacitors.

1.4 External Components

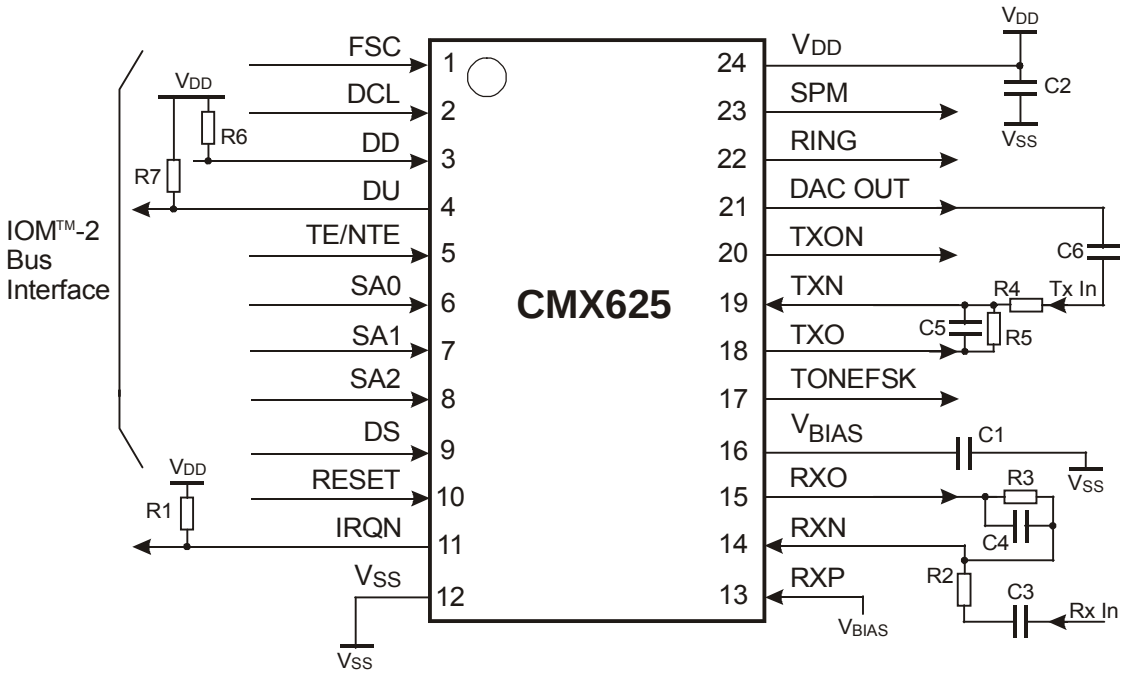


Figure 2 Recommended External Components

R1, R4	100kΩ	C1, C2	1.0µF
R2, R3	110kΩ	C3	100nF
R5	56kΩ	C4, C5	220pF
R6, R7	Note 2	C6	22nF

Resistor ±1%, capacitors ±5% unless otherwise stated.

Note:

1. The recommended component values, C3 to C6 and R2 to R5 and tolerances are essential to meet the ITU-T Recommendation G.172 filter specification. See figure 12.

2. R6, R7 = 750Ω with 5V supply. R6, R7 = 470Ω with 3.3V supply.

1.5 General Description

The CMX625 is a telecom tone generator, DTMF tone encoder/decoder and PCM Codec-Filter for ISDN interfaces. The PCM Codec-Filter performs voice digitisation and reconstruction and incorporates encoder bandpass and decoder lowpass filters with pre and post-filtering with selectable A-law and μ-law companding following ITU-T recommendation G.711. The device has separate output ports for the four different classes of signals encoded. These include Ringing signals, In-band tones or FSK data at 1200bps, high frequency metering pulses (SPM tones) and DAC signals. It has a transmit level attenuator for In-band tones or FSK data and an envelope control for SPM tones. The device also has an uncommitted Tx output buffer for filtering and impedance matching. The functions are controlled via an IOM-2 serial bus interface.

Frequency and timing accuracy of the CMX625 is supplied by the Data Clock (DCL) of the IOM-2 serial bus interface. If the bus is deactivated, DCL is held in a low state.

The CMX625 can be reset externally by driving the RESET pin low. It resets all the internal register bits and ensures that the interface always starts from a known state. The device can also be reset by issuing a RESET command. See section 1.5.14. Commands to enable and disable individual functions are also shown in this section. Approximately 50ms should be allowed for the Tx dc level to settle at V_{BIAS} before enabling the Tx functions (set bit 6 of the MODE Register to '1') after the CMX625 has been reset.

1.5.1 IOM-2 Serial Bus Interface

The IOM®-2 (ISDN Oriented Modular revision 2) is an industry standard serial bus for interconnecting telecommunications IC's. (Refer to the IOM-2 Interface Reference Guide, Industry Standard Bus by Advanced Micro Devices). The bus is an evolution of the IOM® interface and is also known as the GCI (General Circuit Interface).

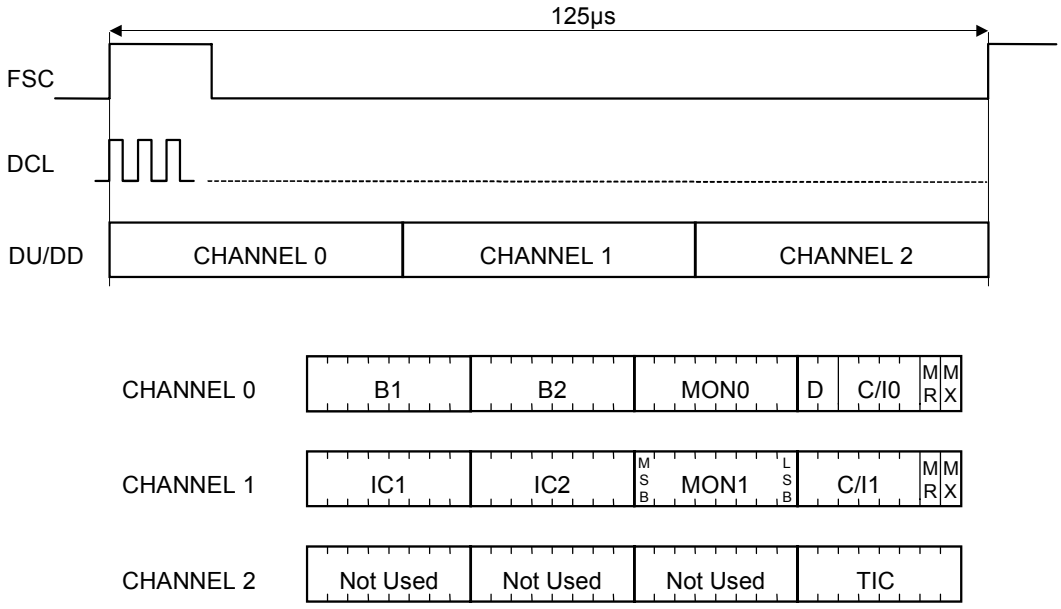
The IOM-2 bus provides a symmetrical full duplex communication link, containing user data, control/programming and status channels. There are two basic modes of operation known as Terminal mode (TE mode) and non-Terminal mode (non-TE or Line Card mode). These modes differ in the frame structure and data rate. The frame rate remains at 8kHz for each mode. The CMX625 acts as a timing and control slave to the upstream device.

The various channels are time multiplexed over a basic four wire serial interface, namely FSC, DCL, DD and DU. Frames are delimited by an 8kHz Frame Synchronisation Clock (FSC) which is generated by the upstream device. The Data Clock (DCL) clocks data on and off the bus and runs at either 1.536MHz (TE mode) or 4.096MHz (non-TE mode). It is always generated by the upstream device. Data Downstream (DD) receives data from the network. Data Upstream (DU) transmits data to the network. When the bus is deactivated or when data is not being transmitted, DD and DU is held in a high impedance state. The DD and DU bus are driven by open drain transistors such that all DD's and DU's can be connected together. Bus reversal (in TE mode) allows the DD and DU pins to be both inputs and outputs in the IC1 and IC2 channels. It allows use of the CMX625 with post processing devices that are IOM-2 compliant. When other devices are connected to the IOM-2 bus the three Slot Address pins (SA0, SA1 and SA2) provide a unique address, allowing the CMX625 to be individually addressed. The Device Select pin (DS) allows two CMX625 devices sharing a slot address to be individually addressed in non-TE mode.

The remote digital IOM loopback is enabled when bit 3 of the IOM CONTROL Register is set to '1'. This loops back the data arriving on the IOM-2 bus and sends it back again. Unused bits in the frame structure are ignored if not required by the CMX625. These bits will be set to '1' when the frame is transmitted upstream.

1.5.2 Terminal Mode (TE)

Terminal mode (TE) frame structure consists of 3 channels of 4 bytes each repeated at 8kHz, i.e. 96 bits in 125µs or a data rate of 768kbps. The Data Clock (DCL) operates at twice the data rate, i.e. 1.536MHz. Figure 3 shows the TE mode frame structure.



FSC = 8kHz
DCL = 1.536MHz
DD, DU = 768kbps

Figure 3 Terminal Mode Frame Structure

'Channel 0' is used for passing user data (2B+D channels) and controlling (MON0 and C/I0) the Layer 1 transceiver. Only 'Channel 1' is used by the CMX625. 'Channel 2' is reserved for D channel arbitration.

The 12 byte frame contains the following channels:

(i) The 'B' channels consist of two 64kbps data channels, labelled B1 and B2, and transfer B channel data to and from the network.

(ii) The 'Monitor' channels consist of two programming channels, labelled MON0 and MON1. Each channel consists of 8 bits of data and has two associated pair of handshake bits that control data flow, MX and MR (monitor transmit and receive). The handshake procedure is described in section 1.5.4. The MON1 channel is used for programming and controlling devices attached to the IOM-2 interface. The CMX625 is programmed via the MON1 channel (see section 1.5.15). The MON0 channel is not used. Monitor channel contention is avoided by a "speak when spoken to" system whereby the CMX625 is given a unique address, programmed with the 3 Slot Address pins (SA0 to SA2) and 1 Device Select pin (DS) and only responds when that address is broadcast by the master device (see section 1.5.14). The Monitor channel address byte is shown below:

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MON Channel Address Byte	1	Slot Address SA2	Slot Address SA1	Slot Address SA0	Device Select DS	0	0	0

The CMX625 cannot initiate MON communication directly in a multi-slave application. Each slave must monitor the MON channel for its unique address in the first byte before processing the following command. Each slave can therefore only drive the DU MON channel when specifically requested to by the master.

(iii) The 'D' channel consists of two bits providing 16kbps for carrying D channel user data. This channel is not used by the CMX625.

(iv) The 'Command/Indicate' channels, labelled C/I0 and C/I1, provide real time status information between devices connected via the IOM-2 bus. The C/I0 in channel 0 consists of 4 bits and the C/I1 in channel 1 is 6 bits wide. The C/I0 in channel 0 is not used.

The C/I1 channel is shared by all devices on the IOM-2 bus with no mechanism for determining and resolving contention. If multiple slave devices are expected to drive the C/I1 channel then care must be taken to allocate different bits to each device. An example of C/I1 channel usage would be 6 slave devices each allocated one of the 6 C/I1 bits. When a slave requires attention it asserts its own bit, which is detected by the master as a C/I1 value change (generating a processor interrupt). The processor would then initiate MON1 communications with the appropriate slave and service its request. This is an example of one usage, but the C/I1 bits may be used for any real time command/indicate purpose dependent on system design and number of slaves on the IOM-2 bus.

The C/I1 Channel Output Control Code is encoded as follows (bits 0, 1 and 2 of the IOM CONTROL Register):

C/I1 Channel Output Control Code (IOM Control Register, Bits 2, 1 and 0)	C/I1 Channel Output Bit Content
0 0 0	C/I1 bits 5-0 = all logic '1', i.e. C/I1 output disabled
0 0 1	Interrupt Request (logic '0') on C/I1 bit 0)
0 1 0	Interrupt Request (logic '0') on C/I1 bit 1)
0 1 1	Interrupt Request (logic '0') on C/I1 bit 2) all other bits logic '1'
1 0 0	Interrupt Request (logic '0') on C/I1 bit 3)
1 0 1	Interrupt Request (logic '0') on C/I1 bit 4)
1 1 0	Interrupt Request (logic '0') on C/I1 bit 5)
1 1 1	Status Register bits 7-2 on C/I1 bits 5-0

Code '000' is provided to disable drive of the C/I1 channel for use when multiple slaves have completely utilised the C/I1 channel resource. The Interrupt Mask Register settings are ignored and the C/I1 bits are set to logic '1'.

For codes '001' to '110' a logic '0' (Interrupt Request) is driven onto the appropriate C/I1 bit when the Status Register bits contain an unmasked logic '1' (set by the Interrupt Mask Register). This allows other devices to use the remaining C/I bits for their own purposes. The master device would use the change of the appropriate C/I bit to initiate a Status Register read from the CMX625.

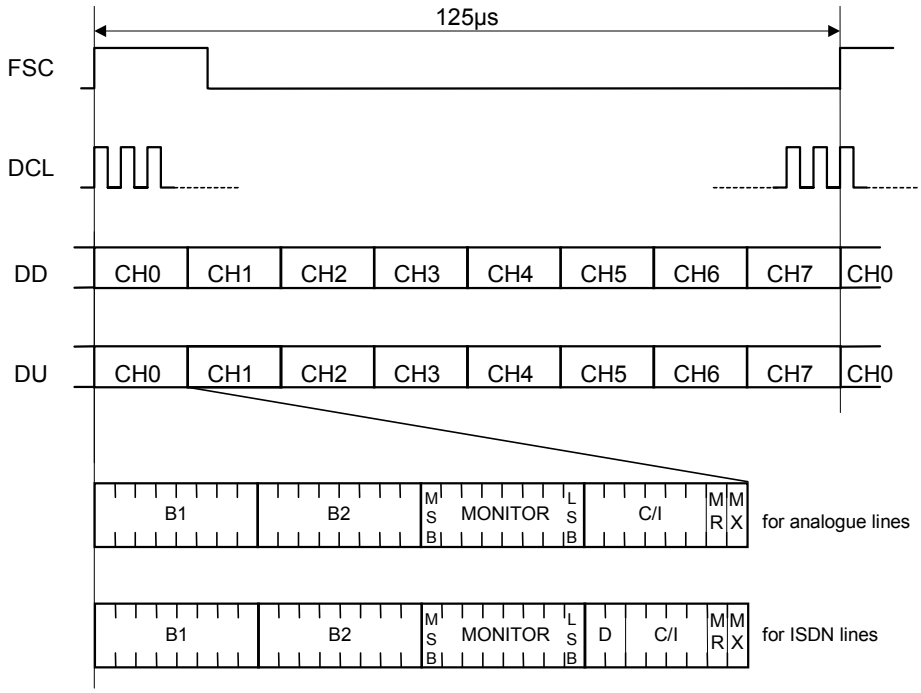
Code '111' and an unmasked Status Register (INTERRUPT MASK bits 2 to 7 are set to '1') allows the most significant 6 bits of the Status Register to be driven onto the C/I1 channel directly for use when the CMX625 is the only slave utilising the C/I channel. If any of the Status bits are masked, by setting the equivalent bit in the mask register to '0', then a logic '0' will be routed to the appropriate C/I1 bit and will not change.

(v) The 'Intercommunication Channel' consists of two 64kbps data channels, labelled IC1 and IC2, and provide additional communications paths between devices other than the layer 1 device (data to and from the layer 1 device is transferred over the B channels).

(vi) The 'TIC' (Terminal IC) bus is used for connecting more than one device to the D and C/I0 channels in Channel 0. The TIC bus is not used by the CMX625.

1.5.3 Non-Terminal Mode (non-TE)

The non-TE mode (Line Card Mode) frame structure consists of up to 8 channels of 4 bytes each repeated at 8kHz, i.e. 256 bits in 125µs or a data rate of 2048kbps for 8 channel frames. The Data Clock (DCL) operates at twice the data rate, i.e. 4.096MHz. Figure 4 shows the non-TE mode frame structure.



FSC = 8kHz
DCL = 4.096MHz
DD, DU = 2048kbps

Figure 4 Non-Terminal Mode Frame Structure

In non-TE mode the IOM-2 bus time multiplexes data, control and status information for up to eight IOM-2 devices or up to 16 Codec-Filters over a single full duplex interface. The frames are subdivided into 8 channels, with one channel being dedicated to each IOM-2 device or pair of Codecs.

Each device on the IOM-2 bus is assigned a slot address and only transmits to and receives from that time slot. Pins SA0, SA1 and SA2 on the CMX625 are used to program the Slot Address. Outside the allocated slot the transmit drivers will be set to high impedance to allow other devices to transmit in their own time slot. To allow two CMX625 devices to share the same slot a Device Select pin (DS) is made available. This pin forms part of the Monitor Channel Address Byte along with the Slot Address pins and allows either of the two devices sharing a slot to be individually addressed. See section 1.5.2, part (ii) MON Channel Address Byte. This mechanism allows both the B1 and B2 data from the same time slot to be utilised by different devices.

Each channel consists of the following 4 bytes:

(i) The first two bytes consist of two 64kbps data channels, labelled ‘B1’ and ‘B2’, and transfer B channel data to and from the network.

(ii) The third byte, labelled ‘Monitor’, is used for programming and controlling devices attached to the IOM-2 interface. The data structure within the monitor channel is not defined and will be device specific. The CMX625 is programmed via the monitor channel (see section 1.5.15).

(iii) In digital applications (ISDN line cards) the fourth byte contains two bits for the 16kbps ‘D’ channel, four ‘Command/Indicate’ (C/I) bits for real time status information and two handshake bits for supporting the handling of the monitor channel, labelled ‘MR’ and ‘MX’ (monitor transmit and receive). The handshake procedure is described in section 1.5.4. In analogue applications (analogue line cards) there is no 'D' channel in the fourth byte so the adjacent C/I channel is increased to 6 bits. The C/I1 channel bits are used in the same way as for Terminal Mode.

1.5.4 Monitor Channel Handshake Protocol

The Monitor channel operates on an event driven basis. While data transfers on the bus take place synchronised to the frame sync, the flow of data is controlled by a handshake procedure using the outgoing MX (monitor transmit) and incoming MR (monitor receive) bits. Data is placed onto the monitor channel and the MX bit is activated. This data will be transmitted repeatedly (once per 8kHz frame) until the transfer is acknowledged (ACK) via the MR bit. The actual data rate is not fixed but is dependent upon the response speed of the transmitter and receiver. The protocol is applicable to both TE and non-TE modes.

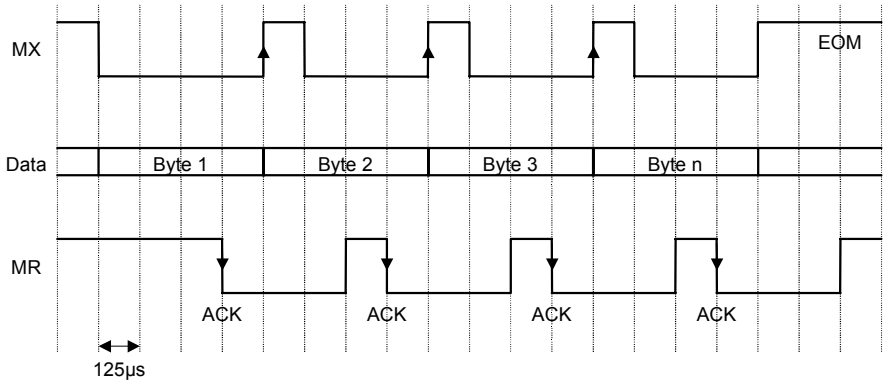
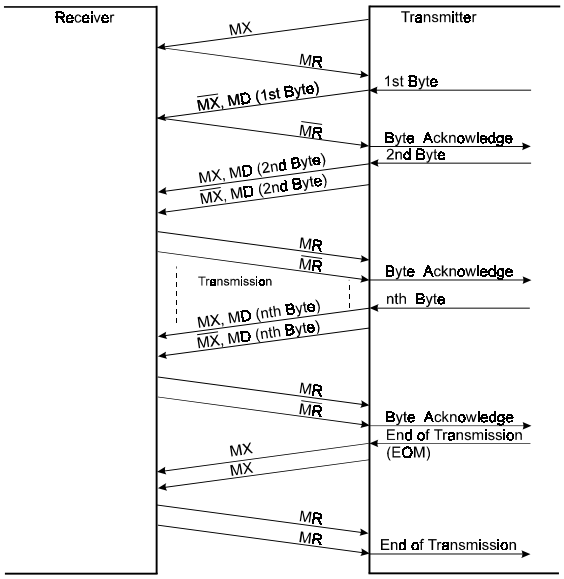


Figure 5 Monitor Handshake Timing (general case)

Figure 5 shows the general case for monitor handshake timing. The first byte of data is placed on the bus and MX is activated (low). MX remains active and the data remains valid until an inactive-to-active transition of MR is received, indicating that the receiver has read the data off the bus. The next byte is placed on the bus after the inactive-to-active transmission of MR, as early as the next frame (there is no limit to the maximum number of frames). At the time that the second byte is transmitted, MX is returned inactive (high) for one frame (MX inactive for more than one frame indicates an End of Message). In response to MX going active (low), MR will be deactivated (high) for one frame (the MX inactive to MR inactive delay can be any number of frames). This procedure is repeated for each additional byte. The transmitter sends an End of Message (EOM), after the last byte of data has been transmitted, by not reactivating MX after deactivating it.

The receiver can hold off the transmitter by keeping MR active until the receiver is ready for the next byte. The transmitter will not start the next transmission cycle until MR goes inactive.
The transmitter is able to abort a transmission by holding MX inactive (high) for two or more frames, this will generate an interrupt when the INTERRUPT MASK Register bit 3 is unmasked (logic ‘1’) and bit 3 of the Status Register will be set to ‘1’.

Figure 6 shows the monitor channel handshake procedure.



MX = Monitor Transmit Bit, active low.
MR = Monitor Receive Bit, active high.
MD = Monitor Data

Figure 6 Monitor Channel Handshake Procedure

Figure 7 shows the maximum speed case for monitor handshake timing. The transmitter can be designed for a higher data throughput than is provided by the general case. The transmitter can deactivate (high) MX and transmit new data one frame after MR is deactivated. In this way, the transmitter is anticipating that MR will be reactivated one frame after it is deactivated, minimising the delay between bytes. MR being held inactive (high) for two or more frames indicates an abort is being signalled by the receiver.

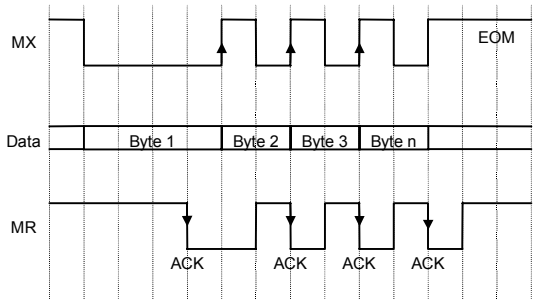


Figure 7 Monitor Handshake Timing (maximum speed case)

The abort is a signal from the receiver to the transmitter indicating that data has been missed. The receiver is able to abort a transmission by holding MR inactive (high) for two or more frames in response to MX going active. An abort from the receiver will generate an interrupt when the INTERRUPT MASK Register bit 2 is unmasked (logic '1') and bit 2 of the Status Register will be set to '1'. Figure 8 shows a monitor abort request from the receiver.

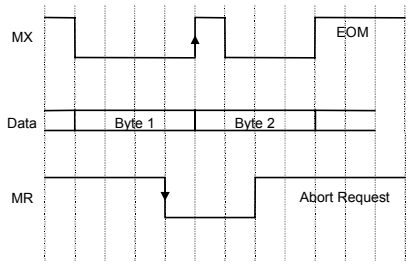


Figure 8 Abort Request from the Receiver

1.5.5 Monitor Channel Identification Command

In order to be able to identify different devices on the IOM-2 bus, an identification command is sent. This allows the software to identify different manufacturer's devices on the bus. The identification sequence is usually done once, when the device is connected for the first time.

A device requesting the identity of a connected CMX625 will transmit the following 2 byte command:

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit 0
DD 1st byte	1	SA2	SA1	SA0	DS	0	0	0
DD 2nd byte	0	0	0	0	0	0	0	0

The CMX625 responds by transmitting:

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit 0	
DU 1st byte	1	SA2	SA1	SA0	DS	0	0	0	Monitor Channel Address Byte
DU 2nd byte	1	0	0	1	1	0	0	1	Device Identification Byte

SA(2-0) = Slot Address, DS = Device Select (see sections 1.5.2 and 1.5.3). See section 1.5.14 for the Device Identification Register.

1.5.6 PCM Codec-Filter

The PCM Codec-Filter performs voice digitisation and reconstruction and incorporates encoder bandpass and decoder lowpass filters with pre and post-filtering with selectable A-law and µ-law companding. In each case the coder and decoder process a companded 8-bit PCM word following ITU-T recommendation G.711 for A-law and µ-law conversion. The encoder bandpass filter and decoder lowpass filter provide passband flatness and stopband rejection according to ITU-T recommendation G.712. The lowpass filter contains the required (Sin X)/X compensation. The overall filter characteristics of the channel are shown in Figure 12.

The PCM Codec-Filter block is enabled or disabled by bit 7 of the CODEC CONTROL Register. The companding law is selected by bit 6. When this bit is a '0', A-law companding is selected (used in Europe) and when this bit is a '1', µ-law is selected (used in the USA and Japan).

The PCM Codec Channel routeing is shown in the table below for normal operation and bus reversal. In 'normal' operation, bit 4 of the IOM Control Register is set to '0', the data is transmitted on the Data Upstream (DU) pin and received on the Data Downstream (DD) pin. Bits 6 and 7 of the IOM Control Register select whether the data is transmitted or received on the B1, B2, IC1 or IC2 channels of the IOM-2 bus. The B1 and B2 channels are available in TE and non-TE mode but the IC1 and IC2 channels are only available in TE mode.

Codec Channel Input/Output Select				
IC Channel Bus Reversal (IOM Control Register Bit 4)		Codec Channel Select (IOM Control Register, Bits 7 and 6)	Codec Data From	Codec Data To
Normal	0	0 0	B1, DD	B1, DU
	0	0 1	B2, DD	B2, DU
	0	1 0	IC1, DD	IC1, DU
	0	1 1	IC2, DD	IC2, DU
Reverse	1	0 0	B1, DD	B1, DU
	1	0 1	B2, DD	B2, DU
	1	1 0	IC1, DU	IC1, DD
	1	1 1	IC2, DU	IC2, DD

In Terminal mode (TE) it may also be necessary to transmit on the Data Downstream (DD) pin and receive on the Data Upstream (DU) pin during the IC1 and IC2 time slots. This can be achieved by selecting bus reversal and allows use of the CMX625 with post processing devices, such as speech scramblers, that are IOM-2 compliant. Bus Reversal is enabled when bit 4 of the IOM Control Register is set to '1' and programming the appropriate Codec Channel Select bits 6 and 7 of the IOM Control Register. When bus reversal is active, the master device and any other devices capable of bus reversal, are prohibited from broadcasting in the active IC channel.

Local analogue codec loopback is enabled when bit 5 of the CODEC CONTROL Register is set to '1'. This internally connects the DAC output to the ADC input (the connection to the Rx Amp is broken). Data is loaded and read via the IOM-2 bus using the channels shown in the above table.

1.5.7 Rx Input Amplifier

This amplifier, with suitable external components, is used for adjusting the received signal to the correct amplitude for the DTMF decoder and the PCM analogue-to-digital converter. See Figure 2 Recommended External Components.

1.5.8 Tx Output Buffer

This buffer is enabled by bit 7 of the SETUP register. With suitable external components it can be used for filtering and impedance matching. See Figure 2 Recommended External Components.

1.5.9 Tone/FSK Encoder and Tone Encoder

These blocks are enabled or disabled by bit 6 of the SETUP register. When bit 5 of the MODE Register is set to '1' then these blocks generate FSK signals as determined by bit 0 of the SETUP Register and the Tx data bits from the UART block, as shown in the table below:

SETUP Register Bit 0	Tone/FSK Generator	FSK Signal Frequency '0' (Space)	FSK Signal Frequency '1' (Mark)
0	V23 1200bps FSK	2100Hz	1300Hz
1	Bell 202 1200bps FSK	2200Hz	1200Hz

When bit 5 of the MODE Register is set to '0', these blocks generate single or dual tones from the range shown in the tables on the following pages. Bit 6 of the MODE Register is then used to enable or disable the block's output to the Tx Signal Control, RING and TONEFSK outputs. There are four tone fields addressed by bits 0 and 1 of the MODE Register.

Tone Field 0, MODE Register bit 1 and bit 0 = '0' and '0' respectively.

TX TONES Register Bits 4-7				Frequency	TX TONES Register Bits 0-3				Frequency
D7	D6	D5	D4	(Hz)	D3	D2	D1	D0	(Hz)
0	0	0	0	0 = OFF	0	0	0	0	0 = OFF
0	0	0	1	252.4	0	0	0	1	* 17.1
0	0	1	0	268.7	0	0	1	0	* 20.5
0	0	1	1	285.3	0	0	1	1	* 24.9
0	1	0	0	315.5	0	1	0	0	* 34.1
0	1	0	1	330.5	0	1	0	1	* 41.0
0	1	1	0	375.2	0	1	1	0	* 51.2
0	1	1	1	404.3	0	1	1	1	-
1	0	0	0	468.0	1	0	0	0	262.9
1	0	0	1	495.8	1	0	0	1	293.6
1	0	1	0	520.6	1	0	1	0	348.2
1	0	1	1	548.0	1	0	1	1	392.6
1	1	0	0	562.8	1	1	0	0	1600
1	1	0	1	578.4	1	1	0	1	1633
1	1	1	0	595.0	1	1	1	0	1827
1	1	1	1	612.5	1	1	1	1	587.2

NOTE: * These outputs are routed to the RING digital output instead of the TONEFSK output. Any single tone output level at TONEFSK output is 0dBm.

Tone Field 1, MODE Register bit 1 and bit 0 = '0' and '1' respectively

TX TONES Register Bits 4-7				Frequency	TX TONES Register Bits 0-3				Frequency
D7	D6	D5	D4	(Hz)	D3	D2	D1	D0	(Hz)
0	0	0	0	0 = OFF	0	0	0	0	0 = OFF
0	0	0	1	120	0	0	0	1	330
0	0	1	0	150	0	0	1	0	416
0	0	1	1	154	0	0	1	1	420
0	1	0	0	250	0	1	0	0	425
0	1	0	1	300	0	1	0	1	433
0	1	1	0	350	0	1	1	0	440
0	1	1	1	360	0	1	1	1	450
1	0	0	0	367	1	0	0	0	460
1	0	0	1	375	1	0	0	1	480
1	0	1	0	380	1	0	1	0	500
1	0	1	1	383	1	0	1	1	600
1	1	0	0	400	1	1	0	0	620
1	1	0	1	450	1	1	0	1	720
1	1	1	0	475	1	1	1	0	930
1	1	1	1	480	1	1	1	1	-

Tone Field 2, MODE Register bit 1 and bit 0 = '1' and '0' respectively

TX TONES Register Bits 4-7				Frequency	TX TONES Register Bits 0-3				Frequency
D7	D6	D5	D4	(Hz)	D3	D2	D1	D0	(Hz)
0	0	0	0	0 = OFF	0	0	0	0	0 = OFF
0	0	0	1	700	0	0	0	1	700
0	0	1	0	900	0	0	1	0	900
0	0	1	1	1100	0	0	1	1	1100
0	1	0	0	1300	0	1	0	0	1300
0	1	0	1	1500	0	1	0	1	1500
0	1	1	0	1700	0	1	1	0	1700
0	1	1	1	-	0	1	1	1	-
1	0	0	0	950	1	0	0	0	2100
1	0	0	1	1400	1	0	0	1	2225
1	0	1	0	1800	1	0	1	0	-
1	0	1	1	2130	1	0	1	1	2750
1	1	0	0	697	1	1	0	0	1209
1	1	0	1	770	1	1	0	1	1336
1	1	1	0	852	1	1	1	0	1477
1	1	1	1	941	1	1	1	1	1633

Tone Field 3, MODE Register bit 1 and bit 0 = '1' and '1' respectively

TX TONES Register Bits 4-7				Frequency	TX TONES Register Bits 0-3				Frequency
D7	D6	D5	D4	(Hz)	D3	D2	D1	D0	(Hz)
0	0	0	0	0 = OFF	0	0	0	0	0 = OFF
0	0	0	1	540	0	0	0	1	540
0	0	1	0	660	0	0	1	0	660
0	0	1	1	780	0	0	1	1	780
0	1	0	0	900	0	1	0	0	900
0	1	0	1	1020	0	1	0	1	1020
0	1	1	0	1140	0	1	1	0	1140
0	1	1	1	-	0	1	1	1	-
1	0	0	0	1380	1	0	0	0	1380
1	0	0	1	1500	1	0	0	1	1500
1	0	1	0	1620	1	0	1	0	1620
1	0	1	1	1740	1	0	1	1	1740
1	1	0	0	1860	1	1	0	0	1860
1	1	0	1	1980	1	1	0	1	1980
1	1	1	0	-	1	1	1	0	-
1	1	1	1	-	1	1	1	1	-

1.5.10 SPM Generator

This block operates independently and has its own output pin. It can transmit 12kHz or 16kHz and is controlled by bit 4 of the SETUP Register. Bit 7 of the MODE Register is used to enable or disable this block. The signal has a rise and fall time each of about 4ms. The SPM signal rises from the bias level to 0dBm in 16 steps of ≈2dB magnitude, and falls from 0dBm to bias level in 16 steps of ≈2dB magnitude.

1.5.11 Transmit Signal Control

This block adjusts the amplitude of the FSK transmit signal output level, the level skew between DTMF tones and the signal routing to the output ports.

Output signal levels are proportional to V_{DD}. The nominal output signal levels (at 0dB attenuation and V_{DD} = 5.0V) are:

Single Tone	0dBm
Dual Tone (per tone)	-3dBm
DTMF High Frequency Tone	-3dBm
DTMF Low Frequency Tone	-5dBm
FSK Signal	0dBm

The level attenuator provides for level adjustment from 0dB to -14dB in -2dB steps. The typical level is determined by bits 2 to 4 of the MODE Register as shown in the table below:

MODE Register			Signal Level Adjustment (dB)
Bit 4	Bit 3	Bit 2	
0	0	0	0
0	0	1	-2
0	1	0	-4
0	1	1	-6
1	0	0	-8
1	0	1	-10
1	1	0	-12
1	1	1	-14

The RING signal is a square, trapezoidal or sinusoidal wave. The square and trapezoidal wave have an amplitude of ≈ V_{DD} peak to peak and the sinusoidal wave has an amplitude of ≈ ½ V_{DD} peak to peak. The trapezoidal ringing waveform has a crest factor (CF) of 1.35. Bits 2 and 3 of the SETUP Register select the waveform type as shown in the table below.

SETUP Register		RING Signal Select
Bit 3	Bit 2	
0	0	Square wave
0	1	Trapezoidal wave
1	0	Sinusoidal wave

1.5.12 Tx UART

This block connects the IOM-2 serial bus interface to the FSK Encoder.

The block can be programmed to convert transmit data from 8-bit bytes to asynchronous data characters by adding Start and Stop bits. The transmit data is then passed to the FSK Encoder.

Data to be transmitted should be loaded, via the IOM-2 bus interface, into the TX DATA Register when the Tx Data Ready bit (bit 6) of the STATUS Register goes high. It will then be treated by the Tx UART block in one of two ways, depending on the setting of bit 1 of the SETUP Register:

If bit 1 of the SETUP Register is '0' (Tx Sync mode) then the 8 bits from the TX DATA Register will be transmitted sequentially at 1200bps, lsb (D0) first.
If bit 1 of the SETUP Register is '1' (Tx Async mode) then bits will be transmitted as asynchronous data characters at 1200 bps according to the following format:

One Start bit (Space)
Eight Data bits (D0-D7) from the TX DATA Register, with the lsb (D0) transmitted first
One Stop bit (Mark)

Failure to load the TX DATA Register with a new value when required will result in bit 7 (Tx Data Underflow) of the STATUS Register being set to '1'. If the 'Tx Async' mode of operation is selected then a continuous Mark ('1') signal will be transmitted until a new value is loaded into TX DATA. If the 'Tx Sync' mode is selected then the byte already in the TX DATA Register will be re-transmitted.

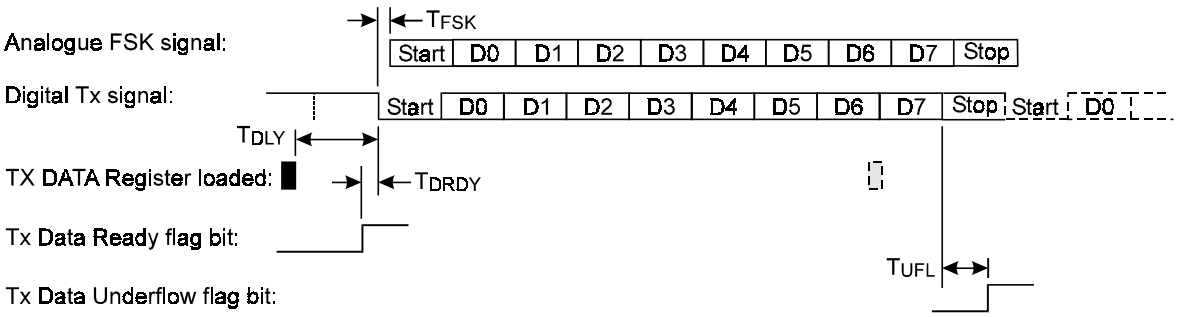


Figure 9a Transmit UART Function (Async)

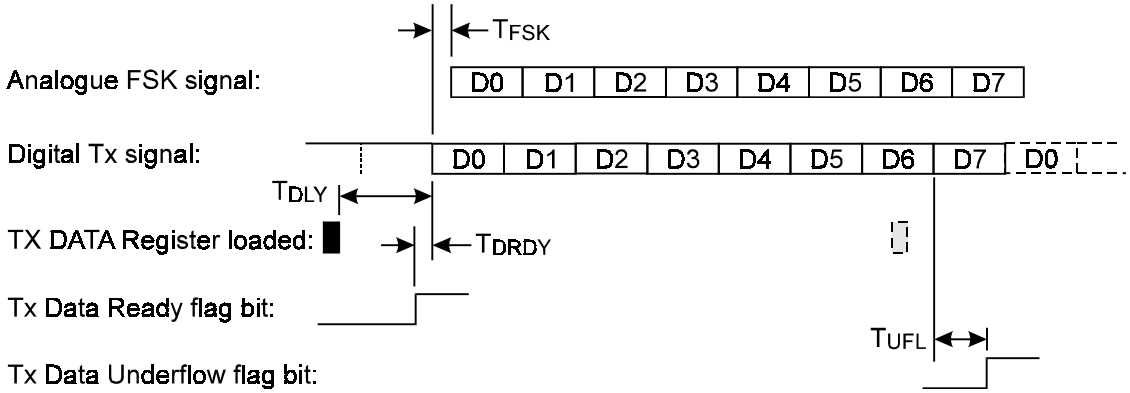


Figure 9b Transmit UART Function (Sync)

1.5.13 DTMF Tone Decoder

This block is enabled or disabled by bit 5 of the SETUP Register. If disabled, bit 4 and 5 of the STATUS Register and bit 0 to bit 3 of the DTMF RX DATA Register are set to '0' and no interrupts are generated.

When bit 5 of the SETUP Register is enabled and bit 4 of the INTERRUPT MASK Register is set to '1' (i.e. unmasked) a 'detected tone' generates an interrupt and bit 4 of the STATUS Register is set to '1'. Reading the STATUS Register clears the IRQN output.

When bit 5 of the SETUP Register is enabled and bit 5 of the INTERRUPT MASK Register is unmasked (logic '1'), a 'status change' of the decoder will generate an interrupt and bit 5 of the STATUS Register will be set to '1'. The validity of the data is indicated by bit 4 of the STATUS Register. The decode truth table is shown below. Reading the STATUS Register clears the IRQN output. An interrupt is not generated when 'no tone' is detected.

DTMF RX DATA Register Bits 0 - 3				DTMF Tone Pairs		
Bit 3 (D3)	Bit 2 (D2)	Bit 1 (D1)	Bit 0 (D0)	Lower Frequency (Hz)	Upper Frequency (Hz)	Keypad Legend
0	0	0	0	941	1633	D
0	0	0	1	697	1209	1
0	0	1	0	697	1336	2
0	0	1	1	697	1477	3
0	1	0	0	770	1209	4
0	1	0	1	770	1336	5
0	1	1	0	770	1477	6
0	1	1	1	852	1209	7
1	0	0	0	852	1336	8
1	0	0	1	852	1477	9
1	0	1	0	941	1336	0
1	0	1	1	941	1209	*
1	1	0	0	941	1477	#
1	1	0	1	697	1633	A
1	1	1	0	770	1633	B
1	1	1	1	852	1633	C

A status change of the decoder and the generation of an interrupt (when the INTERRUPT MASK Register bit 5 is unmasked) will occur both when a tone is first decoded and also when a tone, which was previously present, is no longer decoded. In the latter case, bit 4 of the STATUS Register will be set to '0' to indicate that no tone was detected.

The decoded tone pair is indicated by bits 0-3 in the DTMF RX DATA Register.

1.5.14 Register Set

Write Only Registers

		Data Byte Structure							
Addr.	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$1	RESET	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
$3	SETUP	Tx Output Buffer 0=Disable 1=Enable	Tx Enable 0=Disable 1=Enable	DTMF Rx: 0=Disable 1=Enable	SPM: 0=12kHz 1=16kHz	Ring Signal Select [1]	Ring Signal Select [0]	FSK Mode: 0=Sync 1=Async	FSK Mode: 0=V23 1=Bell 202
$4	MODE	SPM O/P: 0=Disable 1=Enable	Tone/FSK: 0=Disable 1=Enable	Tone/FSK: 0=Tone 1=FSK	Tx Level: MSB	Tx Level:	Tx Level: LSB	Tone Fields: MSB	Tone Fields: LSB
$5	TX DATA	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB
$6	TX TONES	D7 MSB	D6	D5	D4 LSB	D3 MSB	D2	D1	D0 LSB
$8	IOM CONTROL	Codec Channel Select [1]	Codec Channel Select [0]	0	IC Channel Bus Reversal 0=Normal 1=Reverse	Remote Digital IOM Loopback 0=No loopbk 1=Loopback	C/I1 Channel Output Control [2]	C/I1 Channel Output Control [1]	C/I1 Channel Output Control [0]
$9	INT-ERRUPT MASK	Mask Status [7]	Mask Status [6]	Mask Status [5]	Mask Status [4]	Mask Status [3]	Mask Status [2]	0	0
$C	CODEC CONTROL	Codec Enable 0=Disable 1=Enable	PCM Codec: 0=A-Law 1=μ-Law	Local Analogue Loopback 0=No loopbk 1=Loopback	0	0	0	0	0

Read Only Registers

		Data Byte Structure							
Addr.	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$0	DEVICE ID	1	0	0	1	1	0	0	1
$A	STATUS	FSK Mode: FSK Tx Data Underflow	FSK Mode: FSK Tx Data Ready	DTMF Rx: Status Change	DTMF Rx: 1=Detected 0=No Tone Time Out	IOM: Tx Abort	IOM: Rx Abort	0	0
$B	DTMF RX DATA	0	0	0	0	DTMF: Rx Data (D3 MSB)	DTMF: Rx Data (D2)	DTMF: Rx Data (D1)	DTMF: Rx Data (D0 LSB)

Notes:

1. Accessing the RESET Register clears all of the bits in the SETUP, MODE, TX DATA, TX TONES, IOM CONTROL, INTERRUPT MASK, CODEC CONTROL, STATUS and DTMF RX DATA registers and will initialise the device. This a single-byte transaction consisting of the address byte value $1.
2. If any of bits 2, 3, 4, 5, 6 or 7 of the STATUS Register is '1' then the IRQN output will be pulled low when the appropriate bit contains an unmasked logic '1' in the INTERRUPT MASK Register.
3. Reading the STATUS Register clears the IRQN output (when the appropriate bit contains an unmasked logic '1' in the INTERRUPT MASK Register) and also clears all the STATUS Register bits 2 to 7, if set.

1.5.15 Programming the CMX625

The CMX625 is programmed via the 'MON1' (Monitor Channel 1) channel in TE mode and the 'Monitor' channel in non-TE mode. The programming sequence consists of 3 consecutive Monitor bytes: the IOM-2 address, the CMX625 command and data byte. Before executing a command, the CMX625 compares the received IOM-2 address byte with its own address. The MSB of the IOM-2 address is always a '1' (see section 1.5.2). A logical '1' in the MSB of the CMX625 command represents a write operation and a logical '0' represents a read operation.

Structure for Register read/write operations:

IOM Command Register	R/W 0=Read 1=Write	0	X	X	Register Address A3	Register Address A2	Register Address A1	Register Address A0

Example 1: Program the CMX625 to generate interrupt requests for DTMF RX Status Change on bit 5 of C/I channel, i.e. C/I1 Channel Output Control Code (2-0)=110. Set IOM-2 address to SA2-SA0=010 and device select, DS=1.

MX (DD)	MR (DU)	DD (hex)	MX (DU)	MR (DD)	DU (hex)	**Comment**
1	1	FF	1	1	FF	Monitor Channel Idle State
0	1	A8	1	1	FF	Transmit IOM-2 Address
0	0	A8	1	1	FF	Acknowledge Address
1	0	88	1	1	FF	Transmit Command (Write IOM-2 Control, $8)
0	1	88	1	1	FF	
1	0	06	1	1	FF	Acknowledge Command/ Transmit IOM-2 Control Data
0	1	06	1	1	FF	
1	0	FF	1	1	FF	Acknowledge Data
1	1	FF	1	1	FF	End of Transmission
0	1	A8	1	1	FF	Transmit IOM-2 Address
0	0	A8	1	1	FF	Acknowledge Address
1	0	89	1	1	FF	Transmit Command (Write Mask Register, $9)
0	1	89	1	1	FF	
1	0	20	1	1	FF	Acknowledge Command/ Transmit IOM-2 Control Data
0	1	20	1	1	FF	
1	0	FF	1	1	FF	Acknowledge Data
1	1	FF	1	1	FF	End of Transmission
1	1	FF	1	1	FF	Idle

If the command is a register read then only the address and command bytes are sent. The CMX625 will respond with an IOM-2 Register address byte followed by the read data. The IOM-2 Register address byte consists of the Register address that is being read in the least significant 4 bits and the IOM-2 address (less the device select bit) in the most significant 4 bits.

Example 2: Read the CMX625 DTMF RX DATA register, D3-D0=$A. Set IOM-2 address to SA2-SA0 =100 and device select, DS=0.

MX (DD)	MR (DU)	DD (hex)	MX (DU)	MR (DD)	DU (hex)	Comment
1	1	FF	1	1	FF	Monitor Channel Idle State
0	1	C0	1	1	FF	Transmit IOM-2 Address
0	0	C0	1	1	FF	Acknowledge Address
1	0	0B	1	1	FF	Transmit Command (Write IOM-2 Control, $B)
0	1	0B	1	1	FF	
1	0	FF	0	1	CB	Acknowledge Command/ Send Address
1	1	FF	0	0	CB	Address Acknowledged
1	1	FF	1	0	0A	Send DTMF Read Data
1	1	FF	0	1	0A	
1	1	FF	1	0	FF	Data Acknowledged
1	1	FF	1	1	FF	End of Transmission
1	1	FF	1	1	FF	Idle

1.5.16 Glossary

ADC	Analogue to Digital Converter
CIDCW	Caller Identification During Call Waiting
CODEC	Coder/Decoder
DAC	Digital to Analogue Converter
DTMF	Dual Tone Multiple Frequency
FSK	Frequency Shift Keying
GCI	General Circuit Interface
IOM-2	ISDN Oriented Modular revision 2
ISDN	Integrated Services Digital Network
ITU	International Telecommunication Union
NTU	Network Termination Unit
PC	Personal Computer
PCM	Pulse Code Modulation
POTS	Plain Old (Analogue) Telephone Service
SPM	Subscriber Pulse Metering
TA	Terminal Adaptor

1.6 Application Notes

When using the Tone/FSK bit (bit 6) of the MODE Register, each tone starts from $V_{BIAS,}$ and returns to V_{BIAS} before ending:

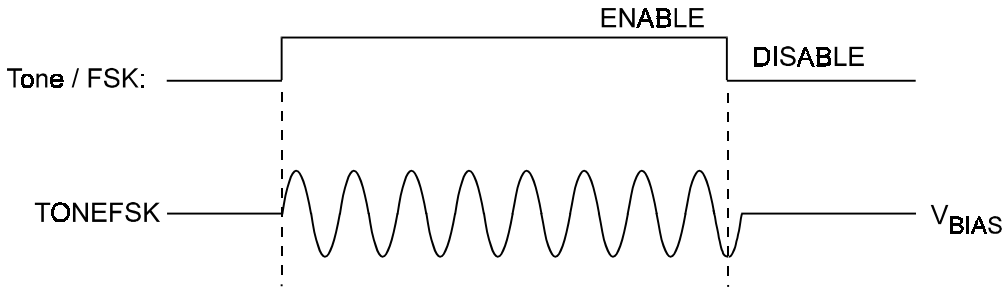


Figure 10 Tone Starting and Stopping

When switching between tones in the same column (bits 4 - 7 or bits 0 - 3) of the TX TONES Register), the transition will be phase continuous. However, switching to the 'OFF' state will immediately take the output of that tone generator to V_{BIAS}.

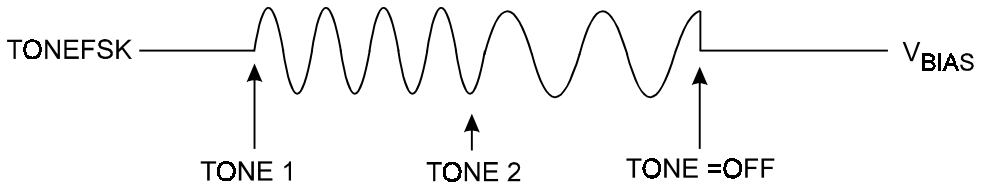


Figure 11 Tone Changing

The TX TONES Register which does not have a frequency allocated is indicated by '-' in the Tone Field tables. These values should not be used.

1.6.1 Telecom Tones

The following tables give the hex codes to be programmed into the particular tone field location for various telecommunications systems applications. The tables are not exhaustive, but list the more commonly used tones.

Ringing Signals

(f ±2.5%) (Hz)	Field 0 (Hex)
Off	$00
16.7	$01
20	$02
25	$03
35	$04
40	$05
50	$06

On Hook 'CPE Alert Tones

Single Tone (Hz)	Field 0 (Hex)
375.2	$60
404.3	$70
468	$80
495.8	$90
520.6	$A0
548	$B0
562.8	$C0
578.4	$D0
1633	$0D

Dual Tone (Hz)	Field 0 (Hex)
375.2+1827	$6E
404.3+1827	$7E
468+1827	$8E
495.8+1827	$9E
520.6+1827	$AE
548+1827	$BE
562.8+1827	$CE
578.4+1827	$DE

NYNEX (MRAA) - AMR Alert Tones (Single Tone)

Group A (Hz)	Field 0 (Hex)
252.4	$10
268.7	$20
285.3	$30
315.5	$40
330.5	$50
375.2	$60

Group B (Hz)	Field 0 (Hex)
468	$80
495.8	$90
520.6	$A0
562.8	$C0
595	$E0
612.5	$F0

Single Frequency Call Progress Tones

(Hz)	Field 1 (Hex)
Off	$00
120	$10
150	$20
154	$30
250	$40
300	$50
350	$60
400	$C0
425	$04
440	$06
450	$07
480	$09
500	$0A
600	$0B
620	$0C

Dual Frequency Call Progress Tones

Additive Mixing (Hz)	Field 1 (Hex)
Off	$00
350+440	$66
440+480	$F6
480+620	$FC
400+425	$C4
400+450	$C7
425+450	$D4
425+480	$F4
120+620	$1C
150+450	$27

Multiplicative Mixing (Hz)	Field 1 (Hex)
400*16.2	$B2
400*20	$A3
400*25	$94
400*33	$85
400*40	$76
400*50	$67
450*25	$E4
600*120	$FD

Dual Tone Multi Frequency Generation

(Hz)	Field 2 (Hex)
Off	$00
941+1633	$FF
697+1209	$CC
697+1336	$CD
697+1477	$CE
770+1209	$DC
770+1336	$DD
770+1477	$DE
852+1209	$EC
852+1336	$ED
852+1477	$EE
941+1336	$FD
941+1209	$FC
941+1477	$FE
697+1633	$CF
770+1633	$DF
852+1633	$EF

Special Information Tones, Fax and Modem Tones and Customer Premises Alert Tones

(Hz)	Field 2 (Hex)
Off	$00
950	$80
1100	$30
1300	$40
1400	$90
1800	$A0
2100	$08
2225	$09
2130+2750	$BB

ITU-T 'R1' Signalling Tones

(Hz)	Field 2 (Hex)
700+900	$12
700+1100	$13
900+1100	$23
700+1300	$14
900+1300	$24
1100+1300	$34
700+1500	$15
900+1500	$25
1100+1500	$35
1300+1500	$45
700+1700	$16
900+1700	$26
1100+1700	$36
1300+1700	$46
1500+1700	$56

ITU-T 'R2' Signalling Tones

Forward mode (Hz)	Field 3 (Hex)
Off	$00
1380+1500	$89
1380+1620	$8A
1500+1620	$9A
1380+1740	$8B
1500+1740	$9B
1620+1740	$AB
1380+1860	$8C
1500+1860	$9C
1620+1860	$AC
1740+1860	$BC
1380+1980	$8D
1500+1980	$9D
1620+1980	$AD
1740+1980	$BD
1860+1980	$CD

Backward mode (Hz)	Field 3 (Hex)
Off	$00
1140+1020	$65
1140+900	$64
1020+900	$54
1140+780	$63
1020+780	$53
900+780	$43
1140+660	$62
1020+660	$52
900+660	$42
780+660	$32
1140+540	$61
1020+540	$51
900+540	$41
780+540	$31
660+540	$21

1.7 Performance Specification

1.7.1 Electrical Performance

1.7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current into or out of V_{DD} and V_{SS} pins	-50	+50	mA
Current into or out of any other pin	-20	+20	mA

D5 Package	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C	-	550	mW
... Derating	-	9	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

P4 Package	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C	-	800	mW
... Derating	-	13	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

1.7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply (V_{DD} - V_{SS})		2.7	5.5	V
Operating Temperature		-40	+85	°C

1.7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
V_{DD} = 2.7V at Tamb = 25°C and V_{DD} = 3.0V to 5.5V at Tamb = -40 to +85°C,
0dBm = 775mVrms = 0dBm0.

DC Parameters		Notes	Min.	Typ.	Max.	Unit
I_{DD}	All Enabled, V_{DD} = 5.0V	1	-	6.9	-	mA
	All Disabled, V_{DD} = 5.0V	1	-	140	-	µA
	DTMF Rx only, V_{DD} = 5.0V	1	-	2.4	-	mA
	Tx (tones, SPM) only, V_{DD} = 5.0V	1	-	3.5	-	mA
	Tx Output Buffer only Enabled, V_{DD} = 5.0V	1	-	1.8	-	mA
	PCM Codec only, V_{DD} = 5.0V	1	-	3.1	-	mA
	All Enabled, V_{DD} = 3.3V	1	-	5.0	-	mA
	All Disabled, V_{DD} = 3.3V	1	-	80	-	µA
	DTMF Rx only, V_{DD} = 3.3V	1	-	1.6	-	mA
	Tx (tones, SPM) only, V_{DD} = 3.3V	1	-	2.3	-	mA
	Tx Output Buffer only Enabled, V_{DD} = 3.3V	1	-	1.3	-	mA
	PCM Codec only, V_{DD} = 3.3V	1	-	2.3	-	mA
Logic '1' Input Level (CMOS inputs)		3	70%	-	-	V
Logic '0' Input Level (CMOS inputs)		3	-	-	30%	V
Logic Input Leakage Current (Vin = 0 to V_{DD})		3	-1.0	-	+1.0	µA
Logic '1' Input Level (TTL inputs)		3	2.0	-	-	V
Logic '0' Input Level (TTL inputs), Vdd = 3.3V-5.5V		3, 13	-	-	0.8	V
Output Logic '1' Level DD, DU (I_{OH} = 4mA)		14	0.8	-	-	V_{DD}
Output Logic '0' Level DD DU (I_{OL} = 6mA)		14	-	-	0.4	V
Output Logic '0' Level IRQN (I_{OL} = 3mA)		14	-	-	0.4	V
IRQN O/P 'Off State Current (V_{OUT} = V_{DD})			-	-	1.0	µA

FSK Encoder and Tx UART	Notes	Min.	Typ.	Max.	Unit
Level at TONEFSK pin	4	-1.0	0	1.0	dBm
Twist (Mark level w.r.t. Space level)		-2.0	0	+2.0	dB
Tx 1200bits/sec (V23 mode)					
Baud Rate (set by UART and DCL)		1194	1200	1206	Baud
Mark (Logical 1) Frequency		1297	1300	1303	Hz
Space (Logical 0) Frequency		2097	2100	2103	Hz
Tx 1200bits/sec (Bell 202 mode)					
Baud Rate (set by UART and DCL)		1194	1200	1206	Baud
Mark (Logical 1) Frequency		1197	1200	1203	Hz
Space (Logical 0) Frequency		2197	2200	2203	Hz

TONEFSK Signal Level	Notes	Min.	Typ.	Max.	Unit
Level at TONEFSK pin for:					
Single tone	4	-1.0	0	1.0	dBm
Dual tone (per tone)	4	-4.0	-3.0	-2.0	dBm
DTMF High Frequency Group	4	-4.0	-3.0	-2.0	dBm
DTMF Low Frequency Group	4	-6.0	-5.0	-4.0	dBm
Output Impedance		-	10.0	-	kΩ
Tone frequency resolution		-2.5	-	2.5	Hz
Tone output distortion	5	-	0.8	-	%

DTMF Decoder	Notes	Min.	Typ.	Max.	Unit
Valid input signal levels (each tone of composite signal)	4	-29.0	-	-2.0	dBm
Not decode level (either tone of composite signal)	4	-	-	-40.0	dBm
Twist = High Tone/Low Tone		-9.0	-	10.0	dB
Frequency Detect Bandwidth		±1.8	-	±4.5	%
Dial Tone Tolerance	6	-	-	0	dB
Noise Tolerance	6,7	-	-14	-	dB
Tone Response time	2	-	-	40.0	ms
Tone De-response time	2	-	-	45.0	ms
Tone burst detected	2	40.0	-	-	ms
Tone burst ignored	2	-	20.0	-	ms
Pause length detected	2	40.0	-	-	ms
Pause length ignored	2	-	-	20.0	ms

SPM Signal Level	Notes	Min.	Typ.	Max.	Unit
Level at SPM pin	4, 9	-1.5	0	1.0	dBm
	4, 9, 10	-1.0	0	0.5	dB
Tone frequency accuracy		-14.0	-	14.0	Hz
Tone output distortion	5	-	1.2	-	%
Output Impedance		-	10.0	-	kΩ

PCM Codec-Filter	Notes	Min.	Typ.	Max.	Unit
PCM Codec-Filter					
Passband	8	300	-	3400	Hz
Passband Gain (at 1.02kHz)	8	-	0	-	dB
Passband Ripple (w.r.t. gain at 1.02kHz)	8	-0.5	-	+0.5	dB
Stopband Attenuation	8	-	30.0	-	dB
Group delay					
Absolute		-	-	600	µs
Relative to 1kHz:					
500Hz		-	-	1.5	ms
600Hz		-	-	0.75	ms
2600Hz		-	-	0.25	ms
2800Hz		-	-	1.5	ms
Signal-to-total distortion ratio as a function of input level (1kHz input level):					
-45dBm	11	22.0	-	-	dBp
-40dBm	11	27.0	-	-	dBp
-30dBm	11	33.0	-	-	dBp
0dBm	11	33.0	-	-	dBp
Variation of gain with input level (1kHz input signal)					
-55dBm0		-3.0	-	+3.0	dB
-50dBm0		-1.0	-	+1.0	dB
-40dBm0		-0.5	-	+0.5	dB
+3dBm0		-0.5	-	+0.5	dB
Idle channel noise	11	-	-	-65.0	dBm0p
Output Impedance		-	1.0	-	kΩ

Tx Output Buffer	Notes	Min.	Typ.	Max.	Unit
Buffer output signal swing; Load greater than 500Ω	12	2.2	-	-	Vp-p

Power-Up Timing	Notes	Min.	Typ.	Max.	Unit
Device reset to reliable signal at TXO, TXON, RING, SPM or TONEFSK output pins		-	50.0	-	ms

Notes:

1. At 25°C, not including any current drawn from the CMX625 pins by external circuitry.
2. At nominal signal frequencies and without skew.
3. Excluding IOM-2 serial bus interface pins: FSC, DCL, DD and DU in bus reversal.
4. At V_{DD} = 5.0V, load resistance greater than 40kΩ, signal levels are proportional to V_{DD}.
5. Frequency above 300Hz.
6. Referenced to DTMF tone of lower amplitude.
7. Bandwidth limited: 0 to 3.4kHz Gaussian Noise.
8. See filter response, Figure 12.
9. SPM has a soft rise and fall time of about 4ms. The level changes between V_{BIAS} and 0dBm in 2dB steps, 16 steps per rise and fall. When SPM is disabled, an extra 4ms falling tail end of signal should be taken into consideration.
10. Over the range V_{DD} = 3.3V to 5.5V at Tamb = 25°C.
11. Represents a psophometrically weighted measurement.
12. For each of the TXON (if enabled) and TXO pins, load placed between the pin and V_{DD} / 2, for V_{DD} = 5.0V only.
13. Derate linearly minimum TTL Logic '0' level from 0.8V at Vdd = 3.3V to 0.5V at Vdd = 2.7V.
14. All outputs CMOS levels.

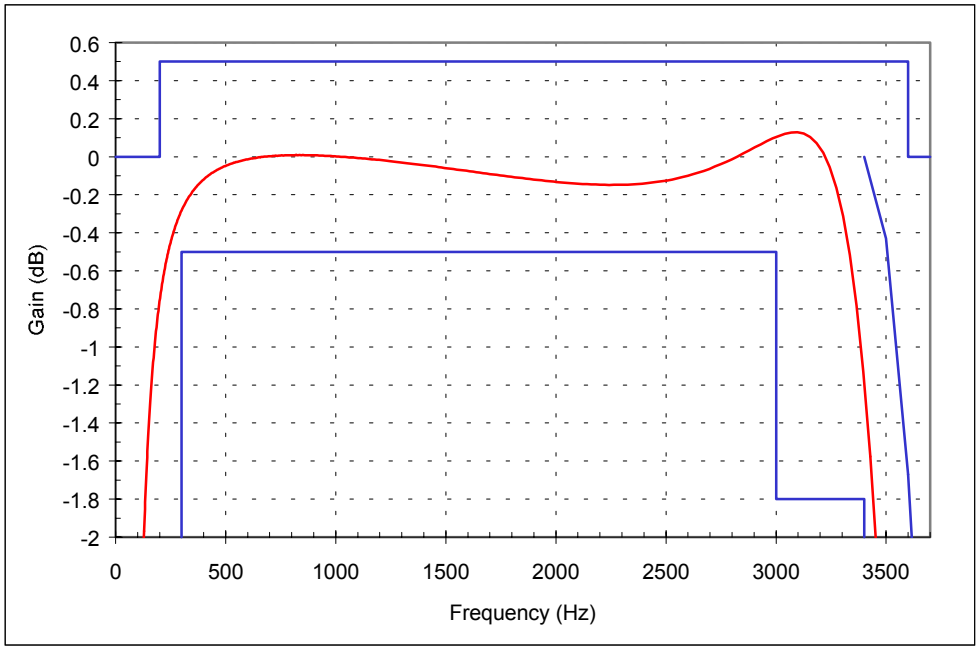


Figure 12a Passband - PCM Codec-Filter overall frequency response

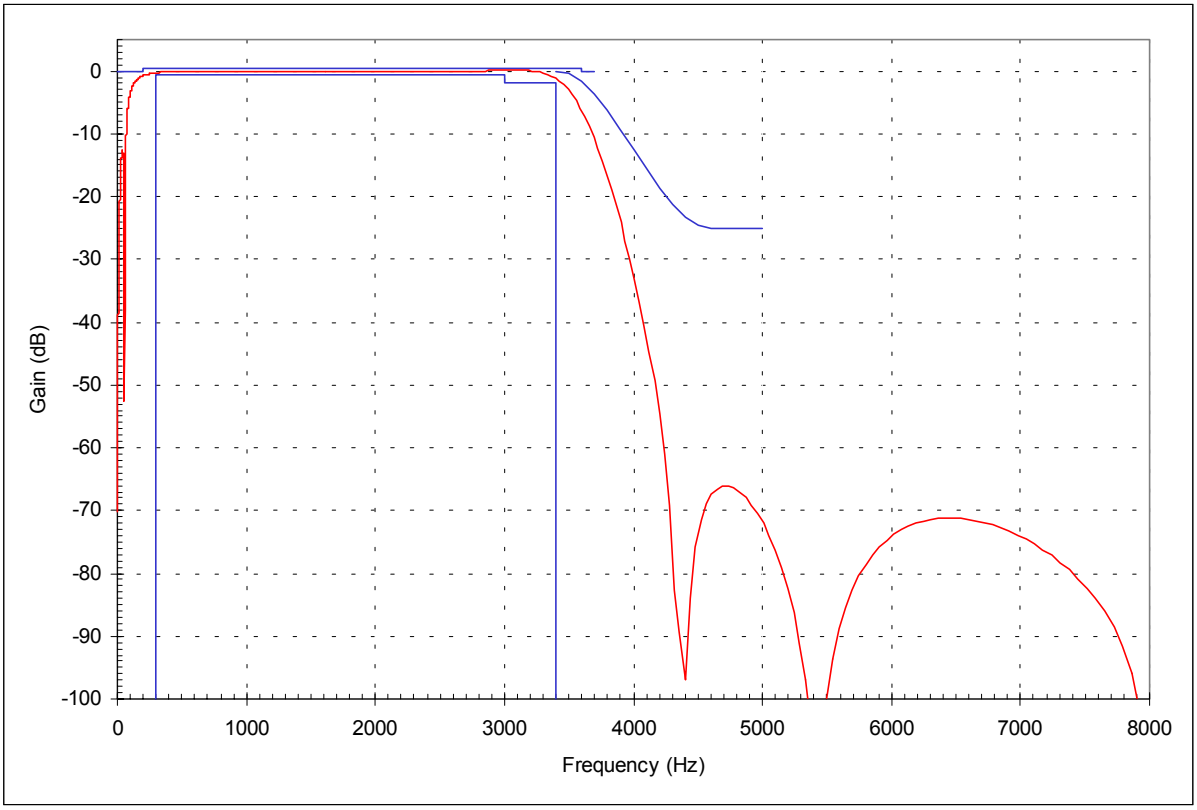


Figure 12b PCM Codec-Filter overall frequency response

	IOM-2 Bus Timing (See Figure 13)	Notes	Min.	Typ.	Max.	Unit
t_{DCL}	DCL clock period in TE Mode	1	-	651	-	ns
t_{DCL}	DCL clock period in non-TE Mode	1	-	244	-	ns
t_R / t_F	DCL clock rise time / fall time	1	-	-	60	ns
FSC	FSC period	1	-	125	-	µs
t_{FSCS}	FSC set-up time	1	70	-	-	ns
t_{FSCH}	FSC hold time	1	40	-	-	ns
t_{DUDC}	DU delay clock (data out)	2	-	-	100	ns
t_{DUDF}	DU delay frame (data out)	2	-	-	150	ns

Notes: 1. These signals are requirements and are not under control of CMX625.
2. Condition C_L = 150pF.

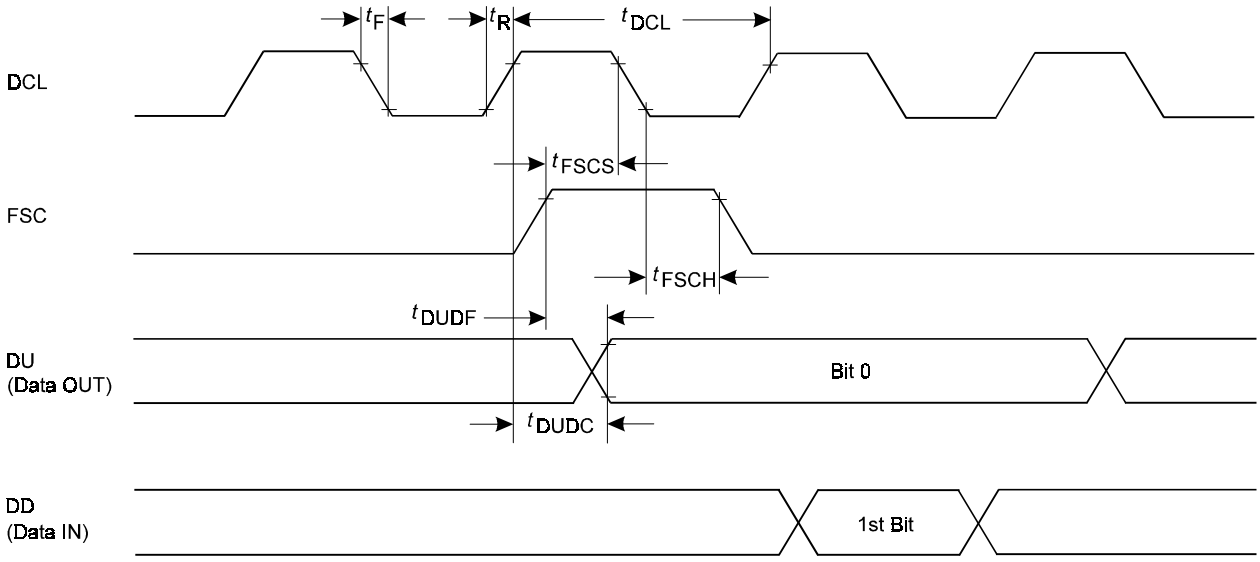
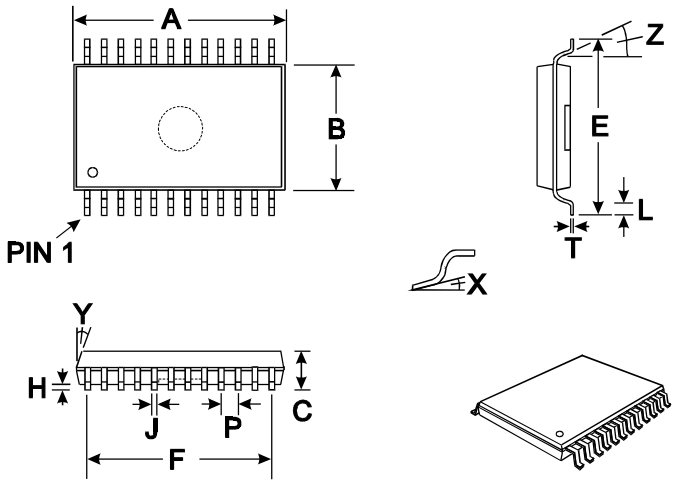


Figure 13 IOM-2 Bus Timing Diagram

	Typical UART Timings (See Figures 9a and 9b)	Notes	Min.	Typ.	Max.	Unit
T_{FSK}	(delay through the modulator)		-	106	-	µs
T_{DLY}	(1 bit period)		-	833	-	µs
T_{DRDY}	(¼ bit-period)		-	208	-	µs
T_{UFL}	(¾ bit-period)		-	625	-	µs

1.7.2 Packaging



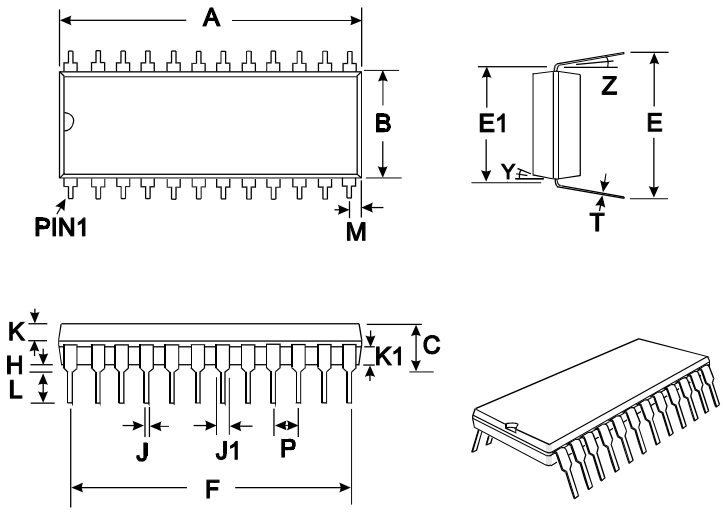
DIM.	MIN.	TYP.	MAX.
* A	0.318 (8.08)		0.328 (8.33)
* B	0.205 (5.21)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
F		0.281 (7.15)	
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.56)		0.037 (0.94)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.23)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 12 24-pin SSOP (D5) Mechanical Outline: *Order as part no. CMX625D5*



DIM.	MIN.	TYP.	MAX.
* A	1.200 (30.48)		1.270 (32.26)
* B	0.500 (12.70)		0.555 (14.10)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
F		1.10 (27.94)	
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.68)		0.074 (1.88)
K1	0.060 (1.52)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.06)
M		0.180 (4.58)	
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	
Z		4°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 13 24-pin DIL (P4) Mechanical Outline: *Order as part no. CMX625P4*

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CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CML Product Data

In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc *(Consumer Microcircuits Limited (UK), MX-COM, Inc (USA) and CML Microcircuits (Singapore) Pte Ltd)* have undergone name changes and, whilst maintaining their separate new names *(CML Microcircuits (UK) Ltd, CML Microcircuits (USA) Inc and CML Microcircuits (Singapore) Pte Ltd*), now operate under the single title **CML Microcircuits**.
These companies are all 100% owned operating companies of the CML Microsystems Plc Group and these changes are purely changes of name and do not change any underlying legal entities and hence will have no effect on any agreements or contacts currently in force.

CML Microcircuits Product Prefix Codes

Until the latter part of 1996, the differentiator between products manufactured and sold from MXCOM, Inc. and Consumer Microcircuits Limited were denoted by the prefixes MX and FX respectively. These products use the same silicon etc. and today still carry the same prefixes. In the latter part of 1996, both companies adopted the common prefix: CMX.

This notification is relevant product information to which it is attached.

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D/CML (D)/1 February 2002